Monolithic InP HEMT V-Band Low-Noise Amplifier

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***Abstract*— A fully monolithic indium phosphide high electron mobility transistor (InP HEMT) two-stage low-noise amplifier has achieved a noise figure of 4.2 dB with an associated gain of 15.25 dB over the band from 56 to 60 GHz. All noise matching and bias decoupling are accomplished on-chip. The successful performance of the amplifier is credited to accurate characterization of the active and passive devices that make up the circuit.**

I. Introduction

INDIUM Phosphide based high electron mobility transistors (InP HEMT's) have demonstrated superior performance as low-noise transistors at frequencies up to 100 GHz [1]–[4]. By empirically matching the discrete InP HEMT's using hybrid circuit techniques, noise figures as low as 0.8 db have been reported with a gain of 9 dB at 60 GHz [1], [2]. A monolithic amplifier with the input matched empirically off chip has also been reported with 3 dB noise figure and 18 dB gain at 63 GHz [5]. However, in order to take advantage of volume production techniques, amplifiers should be completely monolithic. We report here a fully monolithic V-band two-stage low-noise amplifier based on InGaAs–InAlAs–InP HEMT's. Over the band from 56 to 60 GHz, this amplifier has achieved an average noise figure of 4.2 dB and an average gain of 15.25 dB. To our knowledge, these are the best results reported to date for a V-band InP HEMT amplifier that includes on-chip noise matching and on-chip bias decoupling networks.

II. Amplifier Design

The InP HEMT's used in the amplifier had a gate length of 0.15 μm and a total gate width of 48 μm with a unit gate width of 24 μm. Sources were grounded by vias through the 100-μm InP substrate. The HEMT heterostructure was optimized for low-noise operation at V-band [1], [4]. This lattice matched system consists of a superlattice buffer; InGaAs channel; InAlAs spacer, donor, and Schottky layers; and an InGaAs contact layer. Typical dc transconductance is 730 mS/mm with an f_t of 145 GHz. Prior to amplifier design, the noise parameters and S-parameters of individual InP HEMT's were thoroughly characterized to provide a design data base. InP HEMT chips were specially configured to ensure that the characterization is performed in the monolithic circuit environment. The chips included 50-ohm microstrip transmission lines on the InP substrate at both the gate and the drain. Microstrip tapers connected the feed lines to the InP HEMT terminals. The chips were mounted and bonded in packages consisting of 1.85-mm coaxial to microstrip transitions and 50-ohm microstrip feed lines on 0.254-mm thick alumina. This packaging system includes short and offset short calibration pieces that allow accuracy enhanced measurements to the edge of the chip [6]. A standard FET equivalent circuit model [7] was fit to S-parameter data from 12 to 60 GHz using dc resistance measurements for R_{source} and R_{drain}. The InP microstrip lines and tapers were included in the modeling then deembedded prior to amplifier design. This technique yields design data that is accurate in the monolithic circuit environment. Noise parameters were determined in a waveguide measurement system. Like the S-parameters, the noise parameters are also referenced to the gate and drain terminals in the monolithic environment. Passive components used in the amplifier, including capacitors, resistors, coupled lines, and bias networks, were modeled by similar methods. The accuracy of these characterization techniques resulted in a strong basic design. Final performance was achieved by optimizing the bias voltages.

Fig. 1 shows the amplifier chip. The input noise match is accomplished by a series transmission line, an open stub and a second series line. No additional off-chip matching has been used. The interstage network consists of five elements: a series line, an open stub, a coupled line which also provides an interstage dc block, a second open stub, and a second series line. Output matching is provided by a single series line. On both input and output, a short section of 50-ohm line is included for bonding of the chip into the test package. Four bias networks are included on-chip, one for each gate and drain. Each bias network consists of a high impedance transmission line leading to an open stub and a blocking capacitor connected through a channel resistor to ground. This network improves amplifier stability by terminating the transistors in resistive loads out of band.

Design optimization was accomplished using standard commercial design software. During optimization, the length and width of all microstrip lines were allowed to vary simultaneously. The microstrip tapers leading to the gate terminal and from the drain terminal of each InP HEMT were automatically adjusted during optimization to preserve the accuracy of the design. Although the structure of the bias networks was established prior to amplifier design, the placement of the tee connecting the bias network to the circuit was included as part of the optimization.

III. Measured Results

The amplifier was mounted in a coaxial package similar to the one previously described. S-parameters of nine amplifiers were measured to 60 GHz on an automatic vector network

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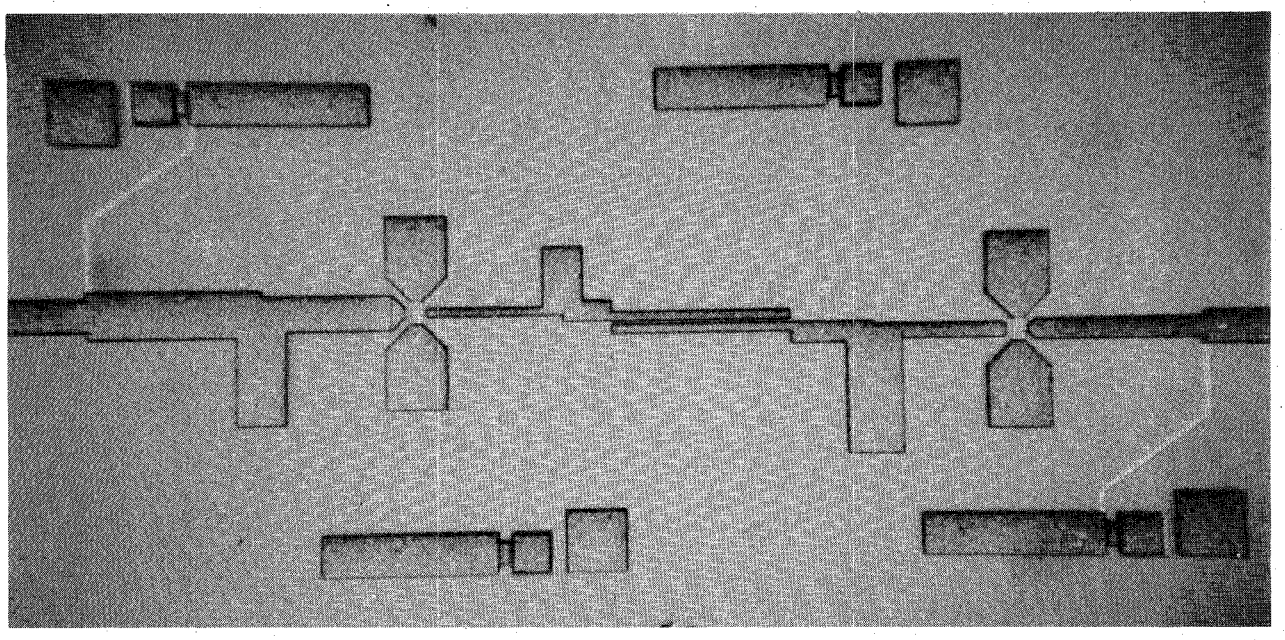

Fig. 1. Photograph of monolithic InP HEMT V-band low-noise amplifier including all matching and bias decoupling on-chip. Chip dimensions are 3.1 × 1.5 mm.

analyzer. Bias lines were joined off-chip so that both transistors were biased to a common drain voltage and to a common gate voltage. No additional off-chip bias decoupling networks were required. Noise figure was determined in the V-band waveguide measurement system using waveguide to coaxial adapters. The noise figure measurements were corrected on a point by point basis for the noise contributed by the waveguide to coaxial and coaxial to microstrip transitions. The loss of the cascaded transitions, from the waveguide port to the edge of the chip, ranges from 0.9 to 1.0 dB across the band of interest.

Fig. 2(a) shows noise figure and associated gain of the amplifier from 56 to 60 GHz. Noise figure across this band is 4.2 dB (+0.7, −1.0 dB) with associated gain of 15.25 dB (+1.3, −2.0 dB). A narrower 56–58-GHz band avoids some slight high frequency rolloff and results in a noise figure of 3.7 dB (± 0.54 dB) and an associated gain of 15.7 dB (± 0.85 dB). For these measurements, V_{drain} = 0.63 V and I_{drain} = 118 mA/mm. Fig. 2(b) shows the input and output return loss under the same bias conditions. The input return loss of 1.5 to 5 dB represents a compromise to achieve low noise across the 4-GHz bandwidth. Keeping the return loss below 5 dB across the band would increase the noise figure by an estimated 1.5 dB. The output return loss of better than 11 dB was achieved with a single series microstrip line. To our knowledge, this is the best performance yet reported for a monolithic InP HEMT V-band low-noise amplifier with on-chip matching and on-chip bias decoupling.

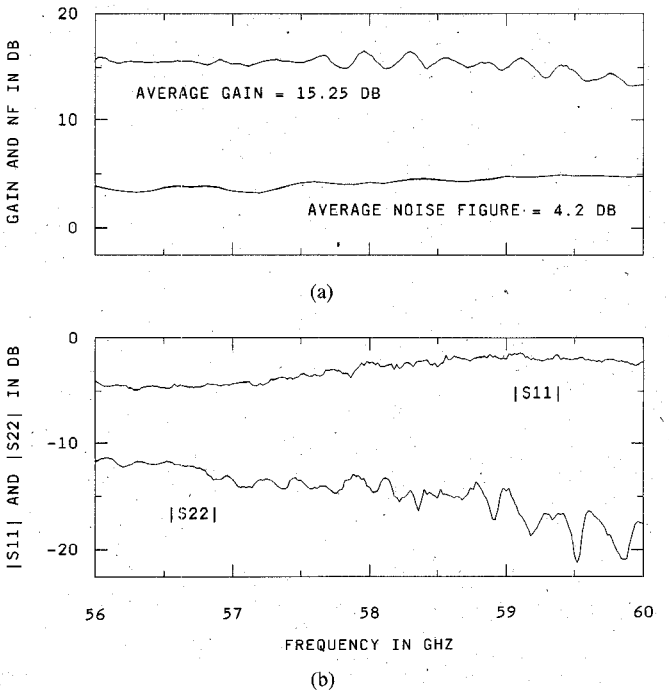

Fig. 2. Experimentally measured performance of monolithic InP HEMT low-noise amplifier. (a) Noise figure and associated gain. (b) Input and output return loss.

IV. Conclusion

A two-stage V-band monolithic low-noise amplifier that exploits the superior performance of InP HEMT's has been demonstrated. Because the amplifier includes all matching and bias decoupling on chip, it requires no empirical tuning. Therefore, the circuit is suitable for further integration with other components to form monolithic subsystems such as transmit/receive modules.

Acknowledgment

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